AMENDMENTS IN THE CLAIMS:

1. (Original) A frequency and phase control apparatus, comprising:

a signal input section for receiving a reproduction signal;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal;

a pattern detection section for detecting a pattern of the binary signal;

a determination section for determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result; and

a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal,

wherein when the determination result of the determination section indicates that the multiple bit digital signal and the clock signal are in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a first state transition rule; and when the determination result of the determination section indicates that the multiple bit digital signal and the clock signal are not in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a second state transition rule.

2. (Original) A frequency and phase control apparatus according to claim 1, wherein:

a number of states and a number of state transition paths of the first state transition rule are restricted based on a first minimum inversion interval defined by a prescribed symbol rule, and

a number of states and a number of state transition paths of the second state transition rule are restricted based on a second minimum inversion interval which is shorter than the first minimum inversion interval.

3. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 2,

the second minimum inversion interval is 1,

the first state transition rule includes 6 states and 10 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR

(a, b, b, a) system, and

the second state transition rule includes 8 states and 16 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, b, a) system.

4. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 1,

the first state transition rule includes 6 states and 8 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, b, a) system, and

the second state transition rule includes 8 states and 16 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, b, a) system.

5. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 2,

the second minimum inversion interval is 1,

the first state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, a) system, and

the second state transition rule includes 4 states and 8 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, a) system.

6. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 1,

the first state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, a) system, and

the second state transition rule includes 4 states and 8 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, a) system.

7. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 2,

the second minimum inversion interval is 1,

the first state transition rule includes 10 states and 16 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, c, b, a) system, and

the second state transition rule includes 16 states and 32 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, c, b, a) system.

8. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 1,

the first state transition rule includes 8 states and 12 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, c, b, a) system, and

the second state transition rule includes 16 states and 32 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, c, b, a) system.

9. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 2,

the first state transition rule includes 6 states and 8 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, b, a) system, and

the second state transition rule includes 6 states and 12 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, b, a) system.

10. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 2,

the first state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a,

b, a) system, and

the second state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, a) system.

11. (Original) A frequency and phase control apparatus according to claim 2, wherein:

the first minimum inversion interval is 3,

the second minimum inversion interval is 2,

the first state transition rule includes 8 states and 12 state transition paths based on a combination of a recording symbol having the first minimum inversion interval and a PR (a, b, c, b, a) system, and

the second state transition rule includes 10 states and 16 state transition paths based on a combination of a recording symbol having the second minimum inversion interval and the PR (a, b, c, b, a) system.

12. (Original) A frequency and phase control apparatus according to claim 1, wherein:

when intervals between a plurality of synchronization patterns included in the detected pattern have a defined value for a prescribed number of times in series, the determination section determines that the multiple bit digital signal and the clock signal are in synchronization with each other, and

when intervals between a plurality of synchronization patterns included in the detected pattern do not have a defined value for a prescribed number of times in series, the determination section determines that the multiple bit digital signal and the clock signal are not in synchronization with each other.

13. (Previously Presented) A frequency and phase control apparatus, comprising:

a signal input section for receiving a reproduction signal;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal;

a maximum cross length detection section for detecting a plurality of cross lengths each representing a length between two adjacent cross points among a plurality of cross points at which the reproduction signal crosses a prescribed slicing level, and detecting a maximum value among sums of two adjacent cross lengths;

a minimum cross length detection section for detecting the plurality of cross lengths and detecting a minimum value among the sums of the two adjacent cross lengths; and

a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the maximum value and the minimum value, and outputting the adjusted clock signal,

wherein the maximum cross length detection section detects the maximum value based on the binary signal.

14. (Previously Presented) A frequency and phase control apparatus according to claim 13, wherein:

the maximum likelihood decoding section generates a binary signal based on a state transition rule, and

a number of states and a number of state transition paths of the state transition rule are restricted based on a minimum inversion interval defined by a prescribed symbol rule.

15. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 2, and

the state transition rule includes 6 states and 10 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b, b, a) system.

16. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 3, and

the state transition rule includes 6 states and 8 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b, b, a) system.

17. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 2, and

the state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b,

a) system.

18. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 3, and

the state transition rule includes 4 states and 6 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b, a) system.

19. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 2, and

the state transition rule includes 10 states and 16 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b, c, b, a) system.

20. (Previously Presented) A frequency and phase control apparatus according to claim 14, wherein:

the minimum inversion interval is 3, and

the state transition rule includes 8 states and 12 state transition paths based on a combination of a recording symbol having the minimum inversion interval and a PR (a, b, c, b, a) system.

21. (Previously Presented) A maximum likelihood decoder for receiving a multiple bit digital signal generated based on a clock signal and a flag indicating whether or not the multiple bit digital signal and the clock signal are in synchronization with each other, and converting the multiple bit digital signal into a binary signal based on the flag, wherein:

when the flag indicates that the multiple bit digital signal and the clock signal are in synchronization with each other, the maximum likelihood decoder generates a binary signal based on a first state transition rule, and when the flag indicates that the multiple bit digital signal and the clock signal are not in synchronization with each other, the maximum likelihood decoder generates a binary signal based on a second state transition rule.

22. (New) A frequency and phase control apparatus, comprising:

a signal input section for inputting a reproduction signal;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal;

a pattern detection section for detecting a pattern of the binary signal;

a determination section for determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result; and

a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal.

23. (New) A frequency and phase control method, comprising the steps of:

inputting a reproduction signal;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

converting the multiple bit digital signal into a binary signal;

detecting a pattern of the binary signal;

determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result; and

adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal.

24. (New) A program for controlling frequency and phase, the program comprising the steps of:

inputting a reproduction signal;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

converting the multiple bit digital signal into a binary signal;

detecting a pattern of the binary signal;

determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result; and

adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal.

25. (New) An apparatus for reproducing information from an information recording medium, the apparatus comprising:

a signal input section for inputting a reproduction signal;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal;

a pattern detection section for detecting a pattern of the binary signal;

a determination section for determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result;

a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal; and

a reproduction section for reproducing information from the information recording medium based on the adjusted clock signal.

26. (New) A method for reproducing information from an information recording medium, the method comprising the steps of:

inputting a reproduction signal;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

converting the multiple bit digital signal into a binary signal;

detecting a pattern of the binary signal;

determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result;

adjusting at least one of a frequency and a phase of the clock signal based on the

detection result and outputting the adjusted clock signal; and

reproducing information from the information recording medium based on the adjusted clock signal.